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PTO/SB/08A (08-00)

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Substitute for form 1449A/PTO  <b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (use as many sheets as necessary)			<b>Complete if Known</b>		
			Application Number	10/743894	
			Filing Date	12/17/2003	
			First Named Inventor	Madurawe, Raminda U.	
			Group Art Unit	2819	
			Examiner Name	D. de	
			Attorney Docket Number		
Sheet	1	of	2		

U.S. PATENT DOCUMENTS						
Examiner Initials*	Cite No. <sup>1</sup>	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code <sup>2</sup> (if known)			
he		4,706,216		Carter	11-10-1987	
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Examiner Initials*	Cite No. <sup>1</sup>	Foreign Patent Document			Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T <sup>2</sup>
		Office <sup>3</sup>	Number <sup>4</sup>	Kind Code <sup>5</sup> (if known)				
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Substitute for form 1449B/PTO  <b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  <i>(use as many sheets as necessary)</i>		Complete if Known	
		Application Number	10/743894
		Filing Date	12/17/2003
		First Named Inventor	Madurawe, Raminda U.
		Group Art Unit	2819
		Examiner Name	D. Le
		Attorney Docket Number	
Sheet	2	of	2

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
he		SEALS & WHAPSHOTT, "Programmable Logic – PLDs and FPGAs", 1997, pp 102-117, McGraw-Hill, USA.	<input type="checkbox"/>
w		ASHOK K. SHARMA, "Programmable Logic Handbook – PLDs, CPLDs, & FPGAs", 1998, pp 99-171, McGraw-Hill, USA.	<input type="checkbox"/>
he		E. AHMED, J. ROSE, "The Effect of LUT and Cluster Size on Deep-Submicron FPGA Performance and Density", FPGA 2000, Monterey, CA, 2000.	<input type="checkbox"/>
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